class mem\_monitor extends uvm\_monitor;

`uvm\_component\_utils(mem\_monitor)

virtual intf vif;

mem\_sequence\_item req;

uvm\_analysis\_port#(mem\_sequence\_item) analysis\_port;

function new(string name = "mem\_monitor",uvm\_component parent);

super.new(name,parent);

endfunction

virtual function void build\_phase(uvm\_phase phase);

super.build\_phase(phase);

uvm\_config\_db#(virtual intf)::get(this,"\*","vif",vif);

analysis\_port = new("analysis\_port", this);

endfunction

virtual task run\_phase(uvm\_phase phase);

req=mem\_sequence\_item::type\_id::create("req");

forever begin

@(vif.mon\_cb);

@(vif.mon\_cb);

req.enable=vif.enable;

req.dina=vif.dina;

req.dinb=vif.dinb;

req.addr=vif.addr;

req.wr=vif.wr;

req.slave\_sel=vif.slave\_sel;

req.dout=vif.dout;

analysis\_port.write(req);

// $display("-----------monitor------------");

// req.print();

end

endtask

endclass